

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Leonard Forbes

Title:

IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY

INSULATORS

Docket No.:

1303.027US1

August 30, 2001

Examiner:

Filed:

Richard A. Booth

Serial No.: 09/945,512

Due Date: N/A

Group Art Unit: 2812

Commissioner for Patents Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

<u>X</u> A return postcard.

<u>X</u> An Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 34 cited references.

Communication Concerning Co-Pending Applications (2 pgs.).

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

Atty: Edward J. Brooks, III

Reg. No. 40,925

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-

6900)

(GENERAL)

PATENT

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Applicant:

Leonard Forbes

Examiner: Richard A. Booth

Serial No.:

09/945,512

Group Art Unit: 2812

Filed:

August 30, 2001

Docket: 1303.027US1

Title:

IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL

BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING CO-PENDING APPLICATION(S)

Commissioner for Patents Washington, D.C. 20231

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Applicant would like to bring to the Examiner's attention the following related copending application(s) in the above-identified patent application:

Serial No.	Filing Date	Attorney Docket	Title	MOM
08/903,453	07/29/1997	303.378US1	GATE INSULATOR FOR SILICO INTEGRATED CIRCUIT TECHN BY THE CARBURIZATION OF	OLOGY
09/651,380	08/29/2000	N/A	THIN DIELECTRIC FILMS FOR STORAGE CAPACITORS	DRAM
09/943,134	08/30/2001	1303.020US1	PROGRAMMABLE ARRAY LO MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BA	
09/945,137	08/30/2001	N/A	LOW COST PROCESSES FOR PRODUCING HIGH QUALITY PEROVSKITE DIELECTRIC FIL	MS
09/945,395	08/30/2001	1303.019US1	DRAM CELLS WITH REPRESS MEMORY METAL OXIDE TUN INSULATORS	
09/945,498	08/30/2001	1303.024US1	DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABL MEMORY WITH INSULATING OXIDE INTERPOLY INSULATO	METAL
09/945,500	08/30/2001	1303.029US1	PROGRAMMABLE MEMORY A AND DECODE DEVICES WITH TUNNEL BARRIER INTERPOL	LOW

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/945,512

Filing Date: August 30, 2001

IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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Dkt: 1303.027US1

FLASH MEMORY WITH LOW TUNNEL 09/945,507 08/30/2001 1303.014US1 BARRIER INTERPOLY INSULATORS **GRADED COMPOSITION GATE** 09/945,514 08/30/2001 1303.015US1 INSULATORS TO REDUCE TUNNELING BARRIERS IN FLASH MEMORY **DEVICES** SRAM CELLS WITH REPRESSED 09/945,554 08/30/2001 1303.028US1 FLOATING GATE MEMORY, METAL

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

OXIDE TUNNEL INTERPOLY

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6913

te ______

Edward J. Brooks, III

Reg. No. 40,925

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